Owners' Manual
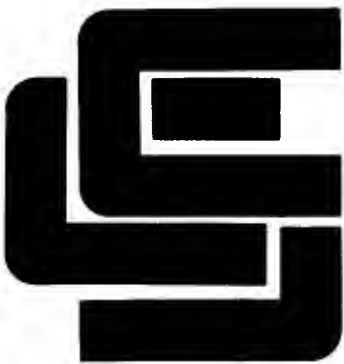
Model 7811 Arithmetic Processor

California Computer Systems

CALIFORNIA COMPUTER SYSTEMS

APPLE II™ ARITHMETIC PROCESSOR UNIT

MODEL 7811B

OWNER'S MANUAL

INTRODUCTION

The CCS 7811B Arithmetic Processor Unit is a powerful floating-point hardware unit which will significantly improve the execution speed of your APPLESOFT II programs. Program execution speeds can be increased by as much as an order of magnitude, depending on how much arithmetic a given program performs, and more sophisticated high-resolution graphics can be produced.

Whenever a speed advantage can be realized, the on-board arithmetic processor performs the APPLESOFT II operations and functions: multiplication, division, the trig functions, inverse tangents, square roots, exponentiation, and natural logarithms. To help you achieve the full power of the 7811B APU, additional functions have been created and are available through the use of the USR(x) function. These include arcsin and arccos of x, the log10 of x, the hyperbolic trig functions, the inverse of x, and pi.

Gaining this increased execution speed involves certain trade-offs. APPLESOFT maintains 8 or 9 significant digits, whereas the 7811B maintains 6 or 7. APPLESOFT gives you a range of approximately $10^{\pm40}$, while the 7811B's range is approximately $10^{\pm20}$. Finally, the 7811B truncates results, whereas APPLESOFT rounds them off. As a result, the slight errors inherent in digital computing will accumulate differently with the 7811B than with APPLESOFT. In most situations the improved speed offered by the 7811B will more than make up for the slight decrease in accuracy.

The 7811B with disk-loaded CCSOFT software is compatible as-is with standard APPLESOFT software. If you have an APPLESOFT ROM Card or APPLE II+, you will need to install a CCSOFT ROM, available separately from CCS. Installation instructions are included as Appendix A of this manual.

SUMMARY OF FEATURES

Uses an AM9511A Arithmetic Processor to Significantly Increase Execution Speeds of APPLESOFT II Arithmetic Operations and Derived Trigonometric and Algebraic Functions

Provides Additional Derived Functions through USR(x)

Provides 32-bit Binary Floating Point and 16-bit or 32-bit Fixed Point Data Formats

Converts Floating Point to Fixed Point and Fixed Point to Floating Point

Supports Interrupt Daisy Chain

Allows DMA Daisy Chain Pass-through

Provides Space for 256-byte Memory Add-on

Uses Glass Epoxy PC Board, Solder-Masked on Both Sides, with Component Silkscreen and Gold-Plated Connectors

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CHAPTER 1

THEORY OF OPERATION

The CCS 7811B, consisting of an AMD AM9511A Arithmetic Processor and the circuitry needed to successfully interface it with the APPLE II, provides high-performance fixed-point and floating-point arithmetic and a variety of floating-point mathematical and trigonometric functions. The specific operations and functions performed are listed in section 1.3 at the end of this chapter. An understanding of the following terms is assumed throughout this manual.

PRECISION: The number of distinct values an operand can represent is a function of its precision. For fixed point data, single-precision refers to 16-bit operands, double-precision to 32-bit operands.

FIXED POINT: The fixed point representation of an operand is a standard binary two's-complement value. The sign (positive=0) is located in the most significant bit (MSB). The range is -32,768 to +32,767 for single-precision and -2,147,483,648 to +2,147,483,647 for double-precision.

FLOATING POINT: The floating point format is analogous to scientific notation; it consists of a mantissa and an exponent expressed in 32 bits. The mantissa is located in the lower 24 bits. The binary point is to the left of bit 23, the MSB, which must be 1

unless the value represented is Zero (which is represented by all 0's). The exponent is represented by bits 24-29. Bit 30 is the exponent sign, bit 31 the mantissa sign (positive=0).

1.1 9511A OPERATION

To perform the operations and derive the functions listed in Section 1.3, the 9511A must be given data, then must be given a command telling it what to do with the data. Data is written to an internal, 16-bit-wide operand stack from which the Arithmetic Logic Unit receives the first operand for an operation. The second operand is supplied from the internal 16-bit bus. The least significant byte of an operand must be pushed onto the operand stack first.

The block diagram below shows the relationships of the main functional parts of the 9511A. The command byte comes across the data bus
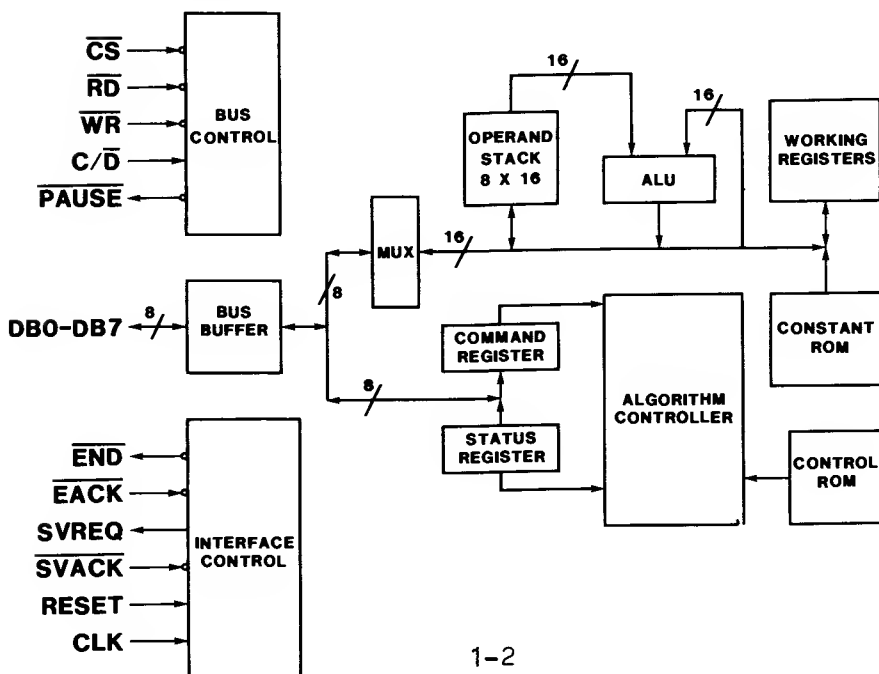
THEORY OF OPERATION

to the Command Register, from which the Microprogram Controller reads it. The microprogram that controls the execution of the command is contained in the Control ROM. The Microprogram Controller causes the program instructions to be sent to the ALU, which carries out the necessary operations. Intermediate results are stored by the ALU in the Working Registers. The constants needed by the ALU to perform the mathematical operations (using Chebyshev Polynomials to minimize and distribute errors) are stored in the Constant ROM. Final results are popped onto the data lines most-significant-byte first.

The 9511A uses the inputs C/-D (Control/-Data), -WR, and -RD to determine the kind of transfer taking place. If C/-D is low, data is either popped from the operand stack onto the data bus (-RD low) or pushed from the data bus onto the stack (-WR low). If C/-D is high, a command is pushed from the data bus into the command register (-WR low), or the status byte is popped from the status register onto the data bus (-RD low).

C/$\overline{D}$	RD	WR	FUNCTION
L	H	L	PUSH DATA BYTE
L	L	H	POP DATA BYTE
H	H	L	ENTER COMMAND BYTE
H	L	H	READ STATUS
X	L	L	UNDEFINED

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Command bytes for the AM9511A have the following format:

```
  σ     Z     ⊢
  Ш     O     ◁
  ∝     ⊢     Σ
  >     ⊢     ∝
  σ     O     O
        Ш     Ⴑ
        ∝
  SVREQ PRECISION FORMAT    OPERATION CODE
```

Bits 0-4 select the operation to be performed. The data format is specified in bit 5: 0 for floating point, 1 for fixed point. Bit 6 controls the precision of the data for fixed point commands, a 1 specifying single-precision (16-bit) operands, a 0 specifying double-precision (32-bit) operands. All floating point operations use 32-bit operands, so if bit 5 is 0, bit 6 must be 0. Results are undefined for all illegal combinations of bits in the command byte.

A 1 in bit 7 causes the 9511A to output a service request after executing the command specified by bits 0-4. Since the 7811B does not use the SVREQ line from the 9511A to communicate with the computer, bit 7 will always be 0.

Status bytes have the following format:

```
  >     Z     O                         >
  σ     O     ∝                         ∝
  ⊃     ⊢     Ш     ERROR CODE          ∝
  ∞     σ     N                         ◁
  BUSY  SIGN  ZERO                      CARRY
```
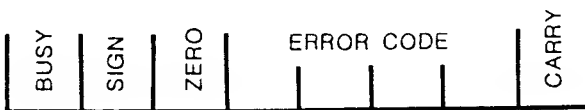
If bit 1 is a 1, the previous operation resulted in a carry or borrow from the most significant bit. Bits 4-1 designate errors according to the following codes:

    0000--No error
    1000--Division by zero
    0100--Square root or log of negative number
    1100--Argument of ACOS, ASIN, or EXP too large
    xx10--Underflow
    xx01--Overflow

THEORY OF OPERATION

Bit 5 is a 1 if the value on the top of the stack
is zero and Bit 6 is 1 if it is negative. If Bit
7 is a 1, the 9511A is executing a command.

1.2 SUPPORT CIRCUITRY

Eight bi-directional data lines are used for
the transfer of data and instructions to and from
the 9511A.   An 8304B bi-directional line buffer
drives the data lines with sufficient power to
ensure successful data transfer, but in doing so
consumes significant amounts of power. As the
driver is not in use most of the time, we have
provided a power-down feature. A transistor
monitors the output of the flip-flop controlled by
-DEV SEL, turning on power for the 8304B only when
-DEV SEL has gone active. The direction of
transfer through the 8304B is controlled by the
R/-W line. The rest of the circuitry is used to
let the 9511A know what to do with incoming data
bytes and to let the CPU know when the 9511A has
completed an operation.

The -RD and -WR inputs of the 9511A are
controlled by the R/-W and -DEV SEL lines from the
APPLE. The R/-W line is inverted and NANDed with
-DEV SEL to control -WR; uninverted, it is NANDed
with -DEV SEL to control -RD. The C/-D input is
controlled directly by address line A0, and the
-CS (Chip Select) input is controlled by -DEV SEL.

Because -DEV SEL remains valid for only half
of one clock cycle and the 9511A requires that the
inputs to -WR, -RD, and -CS remain valid longer
than this (how long depends on the function being
performed), the 7811B includes circuitry designed
to maintain the -DEV SEL signal as long as the
9511A needs it. This is accomplished through the
use of a D-type flip-flop which is clocked by -DEV
SEL. The 9511A also requires that -RD and -WR be
stable before -CS goes active. A sufficient delay
is accomplished by taking the -CS input from the
output of the data buffer transistor, which is
controlled by the Device Select flip-flop.

The 7811B does not need on-board memory, but
sockets are provided for users who wish to add 256
bytes of RAM or ROM. For ROM users, a power-down

feature is included to disable the ROMs when not
in use. The W inputs are permanently disabled.
RAM users must connect the RAM jumper. This
disables the power-down feature (which would
otherwise destroy the contents of the RAM) and
allows the RAM's W inputs to be controlled by the
R/-W line.

The 7811B supports the interrupt daisy chain
and allows DMA daisy chain pass-through. If the
INT jumper is not connected, the interrupt daisy
chain merely passes through the board: INT IN
controls INT OUT. If the jumper is conne   , a
low -END output from the 9511A (signify.   that
the 9511A has completed execution of a command)
pulls INT OUT low, disabling lower-priority
interrupts. The inverted -END output is NANDed
with INT IN to control the -IRQ line. An
interrupt request is thus generated by the 7811B
when -END goes low and INT IN is high (no
higher-priority board generating an interrupt
request).

THEORY OF OPERATION

1.3 9511A COMMAND SUMMARY

COMMAND	DESCRIPTION	CYCLES	CODE
	SINGLE-PRECISION FIXED POINT		
SADD	Add TOS to NOS	16-18	6C
SSUB	Subtract TOS from NOS	30-32	6D
SMUL	Multiply NOS by TOS; Lower result	84-94	6E
SMUU	Multiply NOS by TOS; Upper result	80-98	76
SDIV	Divide NOS by TOS	84-94	6F
	DOUBLE-PRECISION FIXED POINT		
DDAD	Add TOS to NOS	20-22	2C
DSUB	Subtract TOS from NOS	38-40	2D
DMUL	Multiply NOS by TOS; Lower	194-210	2E
DMUU	Mulitply NOS by TOS; Upper	182-218	36
DDIV	Divide NOS by TOS	196-210	2F
	FLOATING POINT		
FADD	Add TOS to NOS	54-368	10
FSUB	Subtract TOS from NOS	70-370	11
FMUL	Multiply NOS by TOS	146-168	12
FDIV	Divide NOS by TOS	154-184	13
	DERIVED FLOATING POINT FUNCTIONS		
SQRT	Square Root of TOS	782-870	01
SIN	Sine of TOS	3796-4808	02
COS	Cosine of TOS	3840-4878	03
TAN	Tangent of TOS	4894-5886	04
ASIN	Inverse Sine of TOS	6230-7938	05
ACOS	Inverse Cosine of TOS	6304-8284	06
ATAN	Inverse Tangent of TOS	4992-6536	07
LOG	Common Logarithm of TOS	4474-7132	08
LN	Natural Logarithm TOS	4298-6956	09
EXP	(e) raised to power in TOS	3794-4878	0A
PWR	NOS raised to power in TOS	8290-12032	0B
	DATA MANIPULATION COMMANDS		
NOP	No operation	4	00
FIXS	Convert TOS from FP to SP format	90-214	1F
FIXD	Convert TOS from FP to DP format	90-336	1E
FLTS	Convert TOS from SP to FP format	62-156	1D
FLTD	Convert TOS from DP to FP format	56-342	1C
CHSS	Change sign of SP operand to TOS	22-24	74
CHSD	Change sign of DP operand to TOS	26-28	34
CHSF	Change sign of FP operand to TOS	16-20	15

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PTOS	Push SP operand on TOS to NOS	16	77
PTOD	Push DP operand on TOS to NOS	20	37
PTOF	Push FP operand on TOS to NOS	20	17
POPS	Pop SP operand from TOS	10	78
POPD	Pop DP operand from TOS	12	38
POPF	Pop FP operand from TOS	12	18
XCHS	Exchange SP operands TOS and NOS	18	79
XCHD	Exchange DP operands TOR and NOS	26	39
XCHF	Exchange FP operands TOS and NOS	26	19
PUPI	Push FP constant PI to TOS	16	1A

NOTES:

1. ABBREVIATIONS:
   TOS = Top of Stack
   NOS = Next on Stack.
   SP = Single-Precision Fixed Point
   DP = Double-Precision Fixed Point
   FP = Floating Point

2. All arithmetic operations and PWR place the result in NOS and then Pop the stack.

3. All derived functions except PWR place the result in TOS.

4. All derived FP functions destroy the contents of the stack. Only the result can be expected to be valid upon command completion.

5. Format conversion commands (FIXS, FIXD, FLTS, FLTD) require that FP data format be specified (command bits 5 and 6 must be 0).

6. NOS becomes TOS in POPS, POPD, POPF comands.

7. For the 7811B, one cycle = 488.9 nanoseconds.

8. All operation codes are hexadecimal values.

CHAPTER 2

INSTALLATION AND CHECKOUT

2.1 BOARD SETUP

If you are going to use CCSOFT, or will not use interrupts or on-board RAM/ROM, the 7811B is complete and ready to be plugged into your computer. No board setup is required and you may proceed to Section 2.2 below.

The 7811B has two jumper-selectable features. If you want the board to generate an Interrupt Request when the 9511A completes a command, solder a jumper into the INT jumper holes. If you are adding RAMs, solder a jumper into the RAM jumper holes. See Chapter 1, "Theory of Operation," for a fuller explanation of these jumper features.

If you decide to add the optional memory to the 7811B, carefully align the memory chips in the sockets (at the left of the board when the connector pins point toward you). Make sure that Pin 1 is in the upper left corner of the chip. Firmly seat the chip in the socket and check for curled or unseated pins. If everything looks fine, you are ready to install the board in your APPLE.

2.2 INSTALLATION

```
******************************************************
*                                                    *
*   WARNING: BEFORE REMOVING THE COMPUTER COVER,      *
*   DISCONNECT THE POWER CORD FROM ITS SOCKET AT      *
*   THE BACK OF THE COMPUTER.   THIS WILL ELIMI-      *
*   NATE THE POSSIBILITY OF ELECTRICAL SHOCK  OR      *
*   DAMAGE TO YOUR COMPUTER.                          *
*                                                    *
******************************************************
```

When the power cord has been disconnected, place the computer in front of you with the keyboard toward you. Place your hands palm-down on the back of the computer cover and curl your fingers around the back edge. Pull until you hear two distinct pops, then stop. Slide the cover to the rear until it is free of the computer and set it aside.

Toward the rear of your computer there are eight 50-pin connectors (usually colored green) with their slots aligned front-to-back. These are the peripheral connectors. They are numbered #0 through #7 from left to right. Slot #0 has special signals on some pins and is reserved for your CCS Model 7114 or other ROM card. The 7811B may reside in any other slot. We recommend that you use slot #1. If you use the CCSOFT ROM, the 7811B must reside in slot #1.

With the gold-plated connector pins pointing down and the component side of the board facing right, carefully align the connector contacts in the peripheral slot you choose. Gently but firmly push down on the card to seat it in the slot, making sure that you seat both the front and back ends of the connector tongue. Replace the computer cover, plug in the power cord, and you are ready to begin testing your new APU.

INSTALLATION AND CHECKOUT

2.3 CHECKOUT

When you turn the power on, watch for any sign of a problem, such as smoke or a funny sound. Such symptoms are rare, but the precaution is nonetheless important. You should hear the familiar beep and see the screen full of question marks. If anything else happens, IMMEDIATELY turn off the power. Disconnect the power cord, remove the computer cover, and make sure that all components are properly seated in their sockets and that the card is seated completely in its slot. Close up the computer and try the power on test again. If the problem persists, see your CCS Dealer.

The next test ensures that the 9511A is functioning. Although far from exhaustive, it tests the ability to enter commands and to read a floating point constant out of the stack. The command is: PUsh PI onto the stack (PUPI). The constant is the internal floating point representation of 3.1415926.

Test 1. Procedure:

        a. Hit reset to initialize stack pointers
        b. Enter "CO91:1A(CR)"
        c. Enter "CO90.CO97(CR)"
        d. The display should show:

        CO90- 02 00 C9 00 0F 00 DA 00

Note that the first, third, fifth, and seventh bytes of step d. are the actual data bytes, while the second, fourth, sixth, and eighth bytes are the 9511A status bytes. This happens because the Command/Data port decoding of the 7811B only goes to the odd/even level within the 16 byte address block assigned to the peripheral connector. Step c. above sequentially accesses 8 of the 16 addresses, resulting in alternate data and status bytes being read and displayed.

CHAPTER 3

INTERFACE SOFTWARE

3.1 INSTALLATION OF CCSOFT

To install the CCSOFT software in your computer, insert the distribution diskette enclosed with your CCS 7811B Arithmetic Processor Unit into your disk drive and do a normal boot of the DOS. Then type in:

        LOAD CCSOFTn (cr)

where n is the number of the slot in which you have installed the 7811B APU module. Now remove the distribution diskette, insert your own initialized diskette, and type in:

        SAVE APPLESOFT (CR)

To use CCSOFT, merely type in:

        FP (cr)

as you normally would. It runs the same as APPLESOFT II does.

Other programs on the diskette include:

BENCH -- A bench mark program

COSHGR -- A demostration program which graphs a hyperbolic cosine in HIRES.

INTERFACE SOFTWARE

> This program runs on either APPLESOFT or CCSOFT. To get a normal text display after running it, type in:

> TEXT (cr)

> Try running it under both APPLESOFT and CCSOFT and note the difference in speed.

3.2   SPECIAL PROGRAMMING NOTES

The AMD 9511A Arithmetic Processing Unit was designed to interface to a different microprocessor than the APPLE's 6502. Additionally, the APPLE itself has a peculiar quirk which, if not compensated for, will cause considerable programming problems with many peripheral chips such as the 9511A. Both of these problems can be compensated for through software.

First, if the 9511A is busy when you attempt to transfer data or commands to it, it will issue a "Not Ready" signal to tell the computer to wait. If the computer is trying to write data to the 9511A, it will ignore this busy signal until after the write operation is complete. In other words, the computer just jams the data in even though the 9511A has indicated that it is not ready. The results are unpredictable.

The solution to this problem is to ensure that the 9511A is not busy BEFORE attempting a write operation. This may be accomplished by reading the 9511A's status and testing Bit 7 for the Busy indication. When Bit 7 is zero the write operation may be performed without harm.

Second, the Apple has a peculiar quirk in it when performing a write operation using indexed addressing: after performing the write operation, it immediately initiates a read cycle. Short of modifying your computer, there is no way to word this secondary read. Since the 9511A is a stack-oriented processor, this write-read operation first puts the data in and pushes the stack down by one byte (write), then pops the stack up by one byte (read). The net effect makes

the stack appear stationary. The only data appearing in the stack is the last written byte.

Two possible solutions exist for this problem. Either don't use indexed addressing, or do a write-push stack one word-read sequence. The first method is easiest to implement but limits your flexibility. Since it involves direct addressing, a different software driver must be written for each slot in which the APU might be installed. This method does improve execution speed. The second method loses speed, but allows for one software driver regardless of slot assignment. This latter method can be implemented with the following code:

```
STA    $C080,x
LDA    #PTOS
STA    $C081,x
LDA    $C080,x
```

where, on entry, A = the data to be written, x = 16 times the slot number, $C080 is the hexadecimal data port base address, $C081 is the hexadecimal command port base address, and PTOS is the 9511A single-precision Push Top Of Stack command.

Note that this problem affects only data write operations. Commands may be written without any need to further adjust the stack.

APPLESOFT II has a command which allows you to create your own assembly language subroutines. This command is the USR(X) function. The APU takes advantage of this to increase the repertoire of functions available to you. Before you can use the USR function, though, you must tell APPLESOFT II where to find the routine. This is done by POKEing the address of the routine into locations 11 and 12 of memory. Then you can treat the USR(X) function as if it were any function. You need not rePOKE the addresses until you want a different function performed.

To POKE the address into memory, issue:

```
POKE 11, (ADDR - 256*INT (ADDR/256))
POKE 12, (INT (ADDR/256)
```

INTERFACE SOFTWARE

Use the following values for ADDR:

FUNCTION	DISKETTE ADDRESS	ROM ADDRESS
ARCSIN(X)	9999	61208
ARCCOS(X)	9994	61204
LOG10(X)	9989	61198
PI	9875	61084
INVERSE(X)	9938	61147
SINH(X)	9959	61166
COSH(X)	9962	61169
TANH(X)	9906	61115

3.3 BENCHMARKS:

Using the CCSOFT software, each floating point function was timed over 5000 repetitions and compared with the APPLESOFT floating point equivalent. The following times were achieved:

FUNCTION	OVERHEAD	CCSOFT	AS II
MUL	11.4 sec	17.6 sec	22.3 sec
FDIV	11.4	17.6	27.3
EXP	13.8	25.4	130.6
SQR	13.8	17.1	248.9
RND	13.8	18.4	29.9
LOG	13.8	26.4	114.3
COS	13.8	26.6	135.2
PWR	11.4	41.1	153.9
TAN	13.8	28.7	244.8
ATN	13.8	29.2	222.4
INT	13.8	16.6	17.1
ACOS	13.8	30.6	554.8
ASIN	13.8	30.4	472.3
LOG(10)	13.8	26.8	325.6
PI	11.4	14.8	53.7
INV	11.4	16.6	29.6
SINH	13.8	37.7	266.5
COSH	13.8	37.4	265.4
TANH	13.8	62.0	403.1

Overhead is the time taken to execute the common code for both CCSOFT and APPLESOFT II. It was obtained using the following program:

```
10 B = 2: C=3
20 FOR I= 1 TO 5000
30 A = B
40 NEXT
50 PRINT "DONE"
```

or the above program with line 30 changed to

```
30 A = ABS(I)
```

Line 30 was then altered to test each function and the program was run under both CCSOFT and APPLESOFT. For example, to test the square root function line 30 was altered to
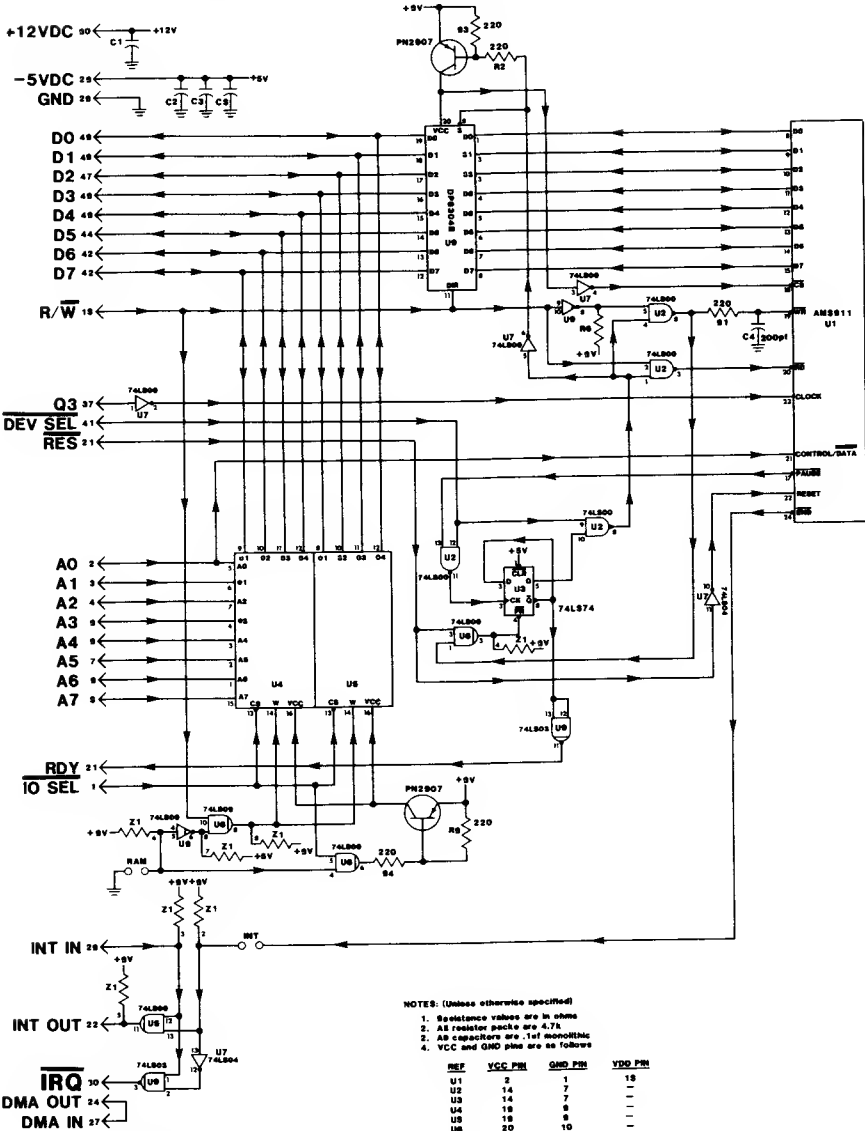
```
30 A = SQR(I)
```

The significant speed advantage of the 7811B is readily apparent.

CHAPTER 4

TECHNICAL INFORMATION

TECHNICAL INFORMATION

4.1 SCHEMATIC/LOGIC DIAGRAM

+12VDC 90
−5VDC 29
GND 28

DO 44
D1 46
D2 47
D3 48
D4 49
D5 45
D6 42
D7 42

R/W̄ 18

Q3 37
DEV S̄EL̄ 41
RES 21

A0 2
A1 3
A2 4
A3 8
A4 8
A5 7
A6 8
A7 8

RDY 21
IO SEL 1

INT IN 28

INT OUT 22

ĪRQ̄ 30
DMA OUT 24
DMA IN 27

NOTES: (Unless otherwise specified)
1. Resistance values are in ohms
2. All resistor packs are 4.7k
3. All capacitors are .1uf monolithic
4. VCC and GND pins are as follows

REF	VCC PIN	GND PIN	VDD PIN
U1	2	1	18
U2	14	7	—
U3	14	7	—
U4	16	8	—
U5	16	8	—
U6	20	10	—
U7	14	7	—
U8	14	7	—
U9	14	7	—

ALU-1
MODEL 7811B
ARITHMETIC PROCESSOR

4-2

TECHNICAL INFORMATION

4.2 PARTS LIST

MODEL 7811B ARITHMETIC PROCESSOR UNIT

ASSY NO. 00000-7811B

#	QTY	REF	CCS P/N	DESCRIPTION
1	4	C1-3,5	42034-21046	CAPACITOR, MONOLYTHIC .1uf, 50vdc
2	1	C4	42215-52715	CAPACITOR, FIXED; MICA 270pf, 500vdc, 10%
3	1	Q1	36100-02907	TRANSISTOR, SI; PNP GENERAL PURPOSE, PN2907
4	5	R1-5	40002-02215	RESISTOR, FIXED, COMP 220 ohm, 1/4W, 10%
5	1	R6	40002-02725	RESISTOR, FIXED, COMP 2.7K ohm, 1/4W, 10%
6	1	U1	31900-09511	IC, DIGITAL, MOS; AM9511 ARITHMETIC PROCESSOR
7	1	U2	30000-00000	IC, DIGITAL, TTL; 74LS00 QUAD 2 IN NAND
8	1	U3	30000-00074	IC, DIGITAL, TTL; 74LS74 DUAL D FLIP FLOP
9	1	U6	30900-08304	IC, DIGITAL, TTL; 8304B OCTAL BUS DRVR/RCVR
10	2	U7	30000-00004	IC, DIGITAL, TTL; 74LS04 HEX INVERTER
11	1	U8	30000-00009	IC, DIGITAL, TTL; 74LS09 QUAD 2 IN AND (OC)
12	1	U9	30000-00003	IC, DIGITAL, TTL; 74LS03 QUAD 2 IN NAND (OC)
13	1	Z1	40930-72726	RESISTOR NETWORK, SIP 2.7K x 7
14	5	XU2,3, 7-9	58102-00140	SOCKET, IC; LOW PROFILE 14 PIN DIP
15	2	XU4,5	58102-00160	SOCKET, IC; LOW PROFILE 16 PIN DIP
16	1	XU6	58102-00200	SOCKET, IC; LOW PROFILE 20 PIN DIP
17	1	XU1	58102-00240	SOCKET, IC; LOW PROFILE 24 PIN DIP
18	1	-	07811-00002	BOARD, PC APU-1, REV B
19	A/R	-	51000-01220	WIRE, BARE; TINNED #22 AWG

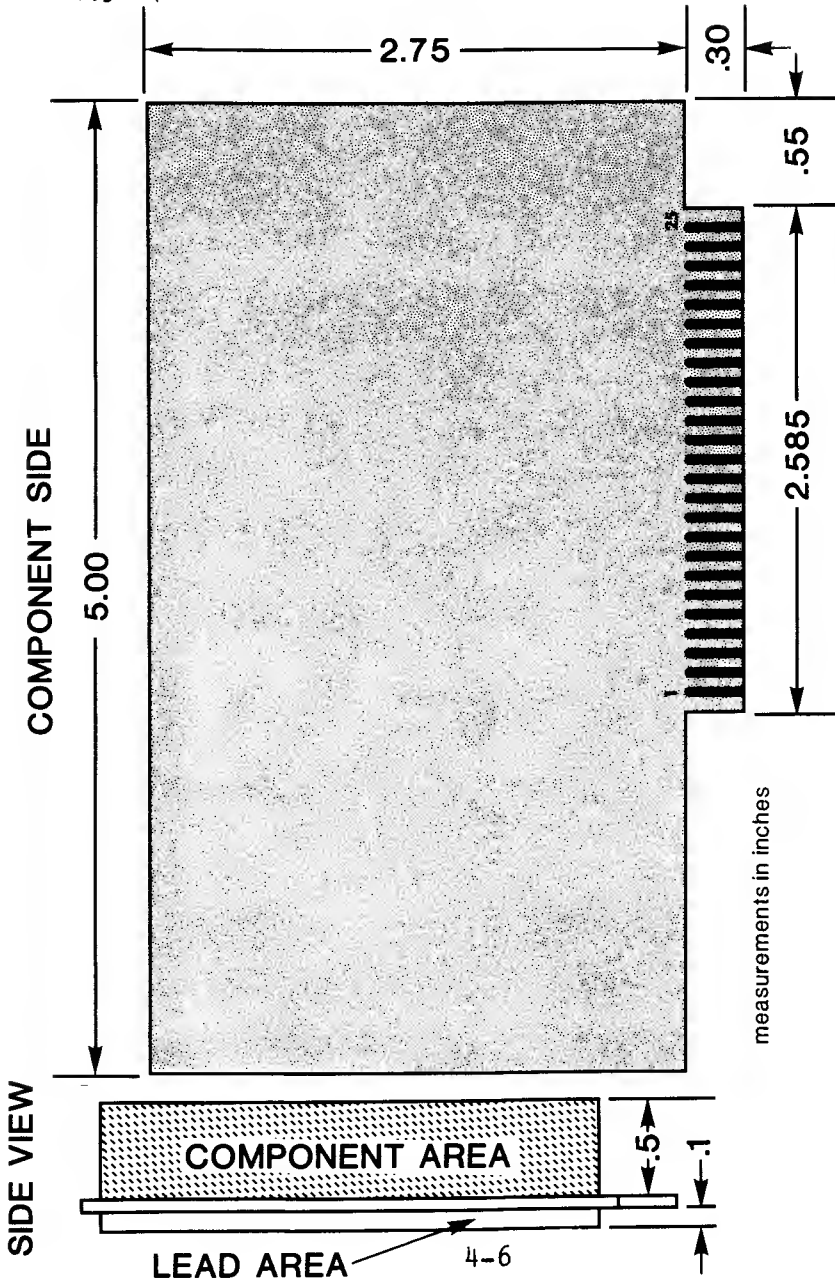## 4.3 ASSEMBLY COMPONENT BREAKDOWN
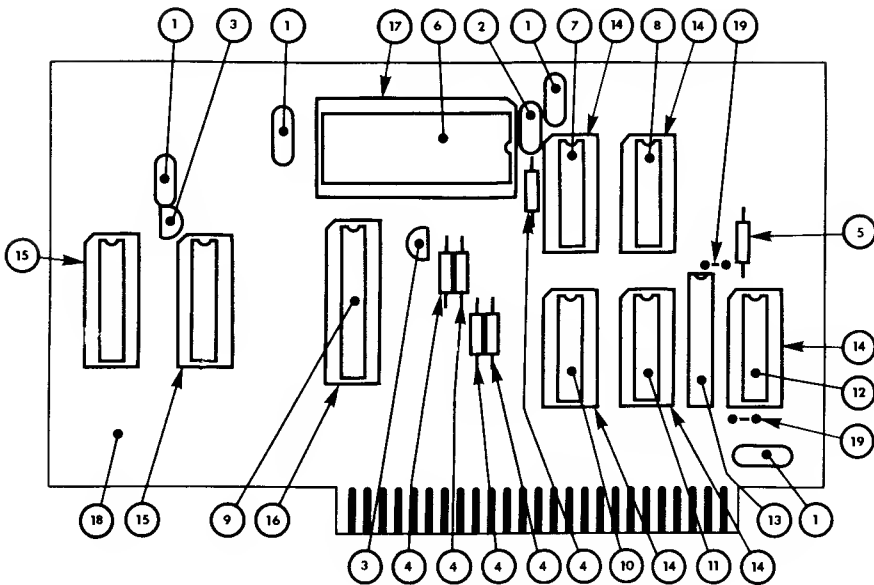
ALL NUMBERS REFERENCE PARTS LIST

4.4 APPLE II I/O CONNECTOR CONFIGURATION

TOP VIEW

BACK OF APPLE

MAIN BOARD

GND	26		25	+5V
DMA IN	27		24	DMA OUT
INT IN	28		23	INT OUT
$\overline{\text{NMI}}$	29		22	$\overline{\text{DMA}}$
$\overline{\text{IRQ}}$	30		21	RDY
$\overline{\text{RES}}$	31		20	$\overline{\text{I/O STROBE}}$
$\overline{\text{INH}}$	32		19	N.C.
-12V	33		18	R/W
-5V	34		17	A15
N.C.	35		16	A14
7M	36		15	A13
Q3	37		14	A12
Φ1	38		13	A11
USER 1	39		12	A10
Φ0	40		11	A9
$\overline{\text{DEVICE SELECT}}$	41		10	A8
D7	42		9	A7
D6	43		8	A6
D5	44		7	A5
D4	45		6	A4
D3	46		5	A3
D2	47		4	A2
D1	48		3	A1
D0	49		2	A0
+12V	50		1	$\overline{\text{I/O SELECT}}$

CIRCUIT SIDE OF PERIPHERAL BOARD

COMPONENT SIDE OF PERIPHERAL BOARD

FRONT OF APPLE

MAIN BOARD

4.5   7811B BOARD DIMENSIONS

measurements in inches

COMPONENT SIDE

5.00

2.75

.30

.55

2.585

SIDE VIEW

COMPONENT AREA

LEAD AREA

.5

.1

4-6

APPENDIX A

THE CCSOFT ROM

A.1 INTRODUCTION

The addition of the CCS 7811B to your system significantly increases the power of your APPLE II. The CCSOFT ROM makes the fast floating-point arithmetic capabilities of the CCS 7811B available to users of the APPLESOFT ROM Card and APPLE II+. Now you can unleash the computational speed of the 7811B upon both pages of high-resolution graphics, increase the functions available to you through easy-to-use USR(x) functions, and speed up most other computational tasks.

This chip may be installed in any of three different ways, depending upon your circumstances and, to some degree, your desires. First, if you have an APPLESOFT Firmware Card, this chip directly replaces one of the ROMs on that card. Second, if you have an APPLE II+, this ROM will directly replace one of the ROMs on the main board of your computer. Last, if you have an APPLE II+ and wish to be able to switch (under software control) between the slightly increased accuracy of the normal APPLESOFT arithmetic and the speed of the 7811B arithmetic, then this ROM may be mounted on a CCS 7114 PROM/ROM Board. In all three cases the 7811B APU must reside in slot #1.

THE CCSOFT ROM

A.2   INSTALLATION AND CHECKOUT

A.2.1   APPLESOFT ROM Card:

a. Place your APPLESOFT ROM Card in front of you with the switch to the right.

b. Just above the top row of chips the numbers 1 to 8 are printed. Carefully remove the chip immediately below the number 4.

c. Orient the CCSOFT ROM chip over the number 4 socket so that Pin 1 is toward the top of the board. The Pin 1 mark will be some sort of notch at the end of the chip or a dot or number in the corner next to Pin 1. If you hold the chip so the writing is right-side-up, Pin 1 should be in the lower left-hand corner.

d. Set the chip down onto the socket, carefully aligning the pins into the socket holes.

e. Firmly but gently seat the chip into the socket.

f. Inspect the chip seating. If any pins are unseated or curled under, carefully remove and reseat the chip.

g. Install the card in your computer as you normally would.

h. Make sure that the CCS 7811B Arithmetic Processor Unit is installed in Slot #1.

i. Close your computer and you are on your way.

A.2.2 APPLE II+:

a. Place your computer in front of you.

b. UNPLUG THE POWER CORD FROM ITS SOCKET AT THE REAR OF YOUR COMPUTER. FAILURE TO DO SO COULD CAUSE ELECTRICAL SHOCK AND/OR DAMAGE TO YOUR COMPUTER.

c. Remove the top cover according to the instructions in your APPLE Reference Manual.

d. About 6 inches from the rear of the computer is a row of 6 larger chips. On the circuit board just in front of the chips are silk-screened circuit designators for the chips. Locate the chip designated ROM-E8.

e. Remove the chip. The ROM itself will be marked 341-0014-00. Place it aside.

f. Orient the CCSOFT ROM over the now-empty socket with Pin 1 toward you. (See II.1.c above for Pin 1 mark identification.)

g. Carefully align the CCSOFT ROM pins into the socket.

h. Firmly but gently seat the chip into the socket.

i. Inspect the chip seating. If any pins are unseated or curled under, carefully remove and reseat the chip.

j. Make sure that your CCS 7811B Arithmetic Processor Unit is installed in Slot #1.

k. Replace the cover on your computer and you are on your way.

THE CCSOFT ROM

A.2.3   APPLE II+ with CCS 7114 PROM/ROM Card:

> a. Place the 7114 PROM/ROM board in front of you with the switch to the right.
>
> b. Observing the Pin 1 mark, align the CCSOFT ROM into the socket labeled E8. (See II.1.c. above for Pin 1 mark identification.)
>
> c. Firmly but gently seat the ROM into the socket.
>
> d. Inspect the ROM seating. If any pins are unseated or curled under, carefully remove and reseat the ROM.
>
> e. Install a 1N4148 or 1N914 diode into the D10 position on the lower left of the board. Be sure to take into account the diode's polarity.
>
> f. Install the 7114 PROM/ROM Card into Slot #0.
>
> g. Make sure the 7811B Arithmetic Processor Unit is in Slot #1.
>
> h. Close up your computer and you are on your way.

A.2.4   Checkout

Testing whether CCSOFT is working is a simple matter. Type in:

?SQR(2)(CR)

Because CCSOFT truncates instead of rounds, it will give a slightly different answer than APPLESOFT. If the result is 1.41421354, CCSOFT is working. If the last digit is a 6 rather than a 4, APPLESOFT is working and something is wrong. Go over the installation procedures to make sure the ROM is properly installed. If improper installation is not the problem, see your dealer.

APPENDIX B

LIMITED WARRANTY

California Computer Systems (CCS) warrants to the original purchaser of its products that

1.) its CCS assembled and tested products will be free from materials defects for a period of one (1) year, and be free from defects of workmanship for a period of ninety (90) days; and
2.) its kit products will be free from materials defects for a period of ninety (90) days.

The responsibility of CCS hereunder, and the sole and exclusive remedy of the original purchaser for a breach of any warranty hereunder, is limited to the correction or replacement by CCS at CCS's option, at CCS's service facility, of any product or part which has been returned to CCS and in which there is a defect covered by this warranty; provided, however, that in the case of CCS assembled and tested products, CCS will correct any defect in materials and workmanship free of charge if the product is returned to CCS within ninety (90) days of original purchase from CCS; and CCS will correct defects in materials in its products and restore the product to an operational status for a labor charge of $25.00, provided that the product is returned to CCS within ninety (90) days in the case of kit products, or one (1) year in the case of CCS assembled and tested products. All such returned products shall be shipped prepaid and insured by original purchaser to:

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LIMITED WARRANTY

Warranty Service Department
California Computer Systems
250 Caribbean Drive
Sunnyvale, California
94086

CCS shall have the right of final determination as to the existence and cause of a defect, and CCS shall have the sole right to decide whether the product should be repaired or replaced.

This warranty shall not apply to any product or any part thereof which has been subject to

(1) accident, neglect, negligence, abuse or misuse;
(2) any maintenance, overhaul, installation, storage, operation, or use, which is improper; or
(3) any alteration, modification, or repair by anyone other than CCS or its authorized representative.

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LIMITED WARRANTY

CCS's obligations under this warranty are conditioned on the original purchaser's maintenance of explicit records which will accurately reflect operating conditions and maintenance preformed on CCS's products and establish the nature of any unsatisfactory condition of CCS's products. CCS, at its request, shall be given access to such records for substantiating warranty claims. No action may be brought for breach of any express or implied warranty after one (1) year from the expiration of this express warranty's applicable warranty period. CCS assumes no liability for any events which may arise from the use of technical information on the application of its products supplied by CCS. CCS makes no warranty whatsoever in respect to accessories or parts not supplied by CCS, or to the extent that any defect is attributable to any part not supplied by CCS.

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